Confirmation No. 7025

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MILANESI	Examiner:	Morris, John J.
Serial No.:	10/563,995	Group Art Unit:	2629
Filed:	January 9, 2006	Docket No.:	DE030240US1 (NXPS.593PA)
Title:	OPERATIONAL AMPLIFIER WITH CONSTANT OFFSET AND APPARATUS COMPRISING SUCH AS OPERATIONAL AMPLIFIER		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed November 16, 2009 and in response to the rejections of claims 1-15 as set forth in the Final Office Action dated May 14, 2009.

Please charge Deposit Account number 50-4019 (DE030240US1) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-15 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated May 14, 2009.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to an apparatus comprising an input stage (*see, e.g.*, input stage 61 shown in Fig. 6, and page 10:14-16) with an NMOS transistor doublet having a first differential input for receiving input signals (*see, e.g.*, transistor doublet N1, N2 shown in Fig. 6, and page 10:20-21), a PMOS transistor doublet having a second differential input for receiving input signals (*see, e.g.*, transistor doublet P3, P4 shown in Fig. 6, and page 10:21-23), and a plurality of switches for receiving and selectively directing analog input signals only to one of either said first differential input or to said second differential input responsive to a switching signal and for connecting the other one of the first and second differential inputs to a reference voltage responsive to the switching signal (*see, e.g.*, switches S1-S8 shown in Fig. 6, and page 10:31 to page 11:17), whereby the input stage is configured to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant (*see, e.g.*, page 7:31 to page 8:5).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-3, 5-10, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) over Huijsing (U.S. Patent No. 4,555,673) in view of Schade (U.S. Patent No. 4,392,112).

B. Claims 4 and 13 stand rejected under 35 U.S.C. § 103(a) over the '673 and '112 references in view of Miyazawa (U.S. Patent Pub. 2002/0196247).

C. Claim 11 stands rejected under 35 U.S.C. § 103(a) over the '673 reference in view of the '112 reference and Applicant Admitted Prior Art (AAPA).

VII. Argument

A. The § 103(a) Rejection Of Claims 1-3, 5-10, 12 and 14-15 Is Improper Because The Cited Combination Of References Does Not Correspond To The Claimed Invention And The '673 Reference Teaches Away From The Proposed Combination.

1. The § 103(a) Rejection Of Claims 1-3, 5-10, 12 and 14-15 Is Improper Because The Cited References Fail To Disclose Selectively Directing Input Signals Only To The Differential Input Of One Of The NMOS And PMOS Doublets.

The cited references do not teach selectively directing input signals only to the differential input of one of the NMOS and PMOS doublets and connecting the differential input of the other one of the NMOS and PMOS doublets to a reference voltage as in the claimed invention. The Examiner acknowledges that the '673 reference does not teach connecting input signals to only one of the differential input portions 20 and 22 (*i.e.,* the asserted NMOS and PMOS doublets) since the '673 reference requires that voltages V_{I+} and V_{I-} be connected to both of the differential input portions 20 and 22. *See, e.g.,* page 2 of the Final Office Action dated May 14, 2009. The '112 reference, however, also fails to teach such aspects. In particular, the '112 reference does not teach NMOS and PMOS doublets that each have a differential input, as erroneously asserted by the Examiner. Instead, the '112 reference teaches that transistors Q3 and Q4 (*i.e.,* one of the asserted doublets) have a common base connection 18 (*i.e.,* these transistor do not have a differential input). *See, e.g.,* Figure 1 and Col. 3:44-53. As the '112 reference does not teach two transistor doublets that each have a differential input, the '112 reference also does not teach connecting one of the differential inputs to input signals and connecting the other (nonexistent) one of the differential inputs to a reference voltage, as in the claimed invention. Because neither reference teaches these aspects of the claimed invention, no reasonable combination of these references can provide correspondence.

In view of the above, the § 103(a) rejection of claims 1-3, 5-10, 12 and 14-15 is improper and Appellant requests that it be reversed.

2. The § 103(a) Rejection Of Claims 1-3, 5-10, 12 and 14-15 Is Improper Because The Cited References Fail To Disclose Keeping The Ratio Of The Transconductances Of Transistor Doublets Constant.

The cited references do not teach keeping the ratio of the transconductance of a NMOS transistor doublet and the transconductance of a PMOS transistor doublet constant. The Examiner has failed to address the claim limitations relating to the ratio of transconductances, and instead the Examiner merely asserted that the '673 reference "teaches constant transconductance" which does not correspond to the claimed invention. Specifically, the '673 reference does not teach keeping the ratio of the transconductances of differential input portions 20 and 22 (*i.e.,* the asserted NMOS and PMOS doublets) constant, as claimed, but instead teaches controlling the transconductance of the differential amplifier that includes the differential input portions 20 and 22. *See, e.g.,* Figure 2. For example, the '673 reference discusses controlling the transconductance of the differential amplifier to be largely constant while failing to make any mention of the transconductances of differential input portions 20 and 22 relative to each other (*i.e.,* the ratio of their transconductances). *See, e.g.,* the Abstract and Col. 2:40-49. As such, there is no correspondence between the '673 reference and the claimed invention. Appellant notes that the '112 reference is not alleged by the Examiner to address the above discussed deficiencies of the '673 reference. Because neither reference teaches these aspects, no reasonable combination of these references can provide correspondence. As such, the § 103 rejection fails.

In a tacit acknowledgement of the lack of express correspondence between the '673 reference and the claimed invention, the Examiner (in the Advisory Action on page 2) appears to assert a theory of inherency. However, the Examiner's assertion is based on mere possibilities in direct violation of M.P.E.P. § 2112. Specifically, the transconductance of one of the differential input portions 20 and 22 of the '673 reference can change relative to the transconductance of the other differential input portion while still maintaining the transconductance of the differential amplifier to be largely constant as taught by the '673 reference. Thus, the ratio of the transconductances of the differential input portions 20 and 22 can change while maintaining the transconductance of the differential amplifier to be constant. As such, there is no inherent correspondence between the '673 reference and the claimed invention. Accordingly, the § 103(a)

rejection of claims 1-3, 5-10, 12 and 14-15 is improper and Appellant requests that it be reversed.

3. The § 103(a) Rejection Of Claims 1-3, 5-10, 12 and 14-15 Is Improper Because The '673 Reference Teaches Away From The Proposed Combination.

The '673 reference teaches away from the Examiner's proposed combination, which would undermine the purpose of the '673 reference. Consistent with the recent *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a §103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('673) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (U.S. 2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.").

In this instance, the '673 reference requires that voltages V_{I+} and V_{I-} (*i.e.,* the asserted input signals) be connected to each of the differential input portions 20 and 22. *See, e.g.,* Figure 2 and Col. 4:12-16 and Col. 4:54 to Col. 5:10. Specifically, the '673 reference requires that the differential input portions 20 and 22 each amplify the input signals in order for the amplifier to function in the intended manner. *See, e.g.,* Col. 3:3-50. Thus, the '673 reference teaches away from connecting the input signals only to one of the differential input portions 20 and 22 and connecting a reference voltage to the other differential input portion, as proposed by the Examiner. Accordingly, there is no motivation for the skilled artisan to modify the '673 reference in such a manner.

In view of the above, the § 103(a) rejection of claims 1-3, 5-10, 12 and 14-15 is improper and Appellant requests that it be reversed.

4. The § 103(a) Rejection Of Claim 3 Is Improper Because The Cited References Fail To Disclose A Plurality Of Switches That Connect The Gates Of Transistors To First And Second Nodes.

The cited references do not teach the arrangement of first, second, third and fourth switches that connect the gates of NMOS and PMOS transistors to first and second nodes as claimed. The Examiner fails to address the manner in which the claimed switches are

arranged, with the cited references merely being asserted by the Examiner to teach switches. Specifically, the Examiner acknowledges that the '673 reference does not teach the claimed switches and the Examiner then asserts that the '112 reference teaches a plurality of switches in Figure 1. Appellant notes that the Examiner fails to indicate which of the switches in Figure 1 of the '112 reference (*e.g.,* S1-S6) allegedly correspond to the claimed first, second, third and fourth switches. Accordingly, the Examiner has failed to establish correspondence to the claimed invention and the rejection necessarily fails.

Appellant further submits that it is readily apparent that the switches in Figure 1 of the '112 reference do not correspond to the switches recited in claim 3. For example, the '112 reference does not teach that the gate of the first of two NMOS transistors of the NMOS doublet is connectable to a first input node via a first switch, with the gate of the first of two PMOS transistors of the PMOS doublet also being connectable to the first input node via a third switch, as in the claimed invention. As another example, the '112 reference does not teach that the gate of the second of the two NMOS transistors is connectable to a second input node via a second switch, with the gate of the second of the two PMOS transistors also being connectable to the second input node via a fourth switch, as in the claimed invention. Because neither reference teaches these aspects of the claimed invention, no reasonable combination of these references can provide correspondence. Appellant further notes that the Examiner acknowledges that the '673 and '112 references do "not teach the gates of the transistors being connected to the same node." Page 6 of the Final Office Action dated May 14, 2009.

In view of the above, the § 103(a) rejection of claim 3 is improper and Appellant requests that it be reversed.

B. The § 103(a) Rejection Of Claims 4 and 13 Is Improper Because The Cited Combination Of References Does Not Correspond To The Claimed Invention And The '673 Reference Teaches Away From The Proposed Combination.

The § 103 rejection of claims 4 and 13 is improper because the cited combination of the '673 and '112 references does not correspond to the claimed invention as discussed above under headings A(1) and A(2). Moreover, the '673 reference teaches away from the Examiner's proposed combination as discussed above under heading A(3). Appellant

notes that the '247 reference is not alleged by the Examiner to address the above discussed deficiencies of the cited combination of the '673 and '112 reference. For at least these reasons, the § 103 rejection of claims 4 and 13 is improper since these claims depend from claim 1. Accordingly, Appellant requests that the § 103 rejection of claims 4 and 13 be reversed.

1. The § 103(A) Rejection Of Claim 4 Is Improper Because The Cited References Fail To Disclose A Plurality Of Switches That Connect The Gates Of Transistors To First And Second Reference Nodes.

The cited references do not teach the arrangement of fifth, sixth, seventh and eighth switches that connect the gates of NMOS and PMOS transistors to first and second reference nodes as claimed. The Examiner acknowledges that the '673 and '112 references do "not teach the gates of the transistors being connected to the same node." Page 6 of the Final Office Action dated May 14, 2009. As such, neither of these references teaches the arrangement of switches recited in claim 4. The Examiner's further reliance upon the '247 reference does not address the deficiencies of '673 and '112 references because the '247 reference does not teach that the gates of the cited transistors (*i.e.,* M5, M6, M2 and M4) are connected to the cited nodes (*i.e.,* phi3 and phi2) via switches. Instead, the '247 reference teaches that the gates of transistors M5 and M6 are connected directly to phi3 and the gates of transistors M2 and M4 are connected directly to phi2. *See, e.g.,* Figure 1. Because none of the cited references teach the arrangement of switches of the claimed invention, no reasonable combination of these references can provide correspondence.

Moreover, claim 4 requires that the gates of the two NMOS transistors are connectable to the first reference node via respective switches and the gates of the two PMOS transistors are connectable to the second reference node via respective switches. The '247 reference, however, teaches that the gates of PMOS transistor M5 and NMOS transistor M6 are connected to phi3 and that the gates of PMOS transistor M2 and NMOS transistor M4 are connected to phi2. Thus, in the '247 reference, the gates of the PMOS transistors are connected to different nodes and the gates of the NMOS transistors are connected to different nodes.

In view of the above, the § 103(a) rejection of claim 4 is improper and Appellant requests that it be reversed.

C. The § 103(a) Rejection Of Claim 11 Is Improper Because The Cited Combination Of References Does Not Correspond To The Claimed Invention And The '673 Reference Teaches Away From The Proposed Combination.

The § 103 rejection of claim 11 is improper because the cited combination of the '673 and '112 references does not correspond to the claimed invention as discussed above under headings A(1) and A(2). Moreover, the '673 reference teaches away from the Examiner's proposed combination as discussed above under heading A(3). Appellant notes that AAPA is not alleged by the Examiner to address the above discussed deficiencies of the cited combination of the '673 and '112 reference. For at least these reasons, the § 103 rejection of claim 11 is improper since these claims depend from claim 1. Accordingly, Appellant requests that the § 103 rejection of claim 11 be reversed.

VIII. Conclusion

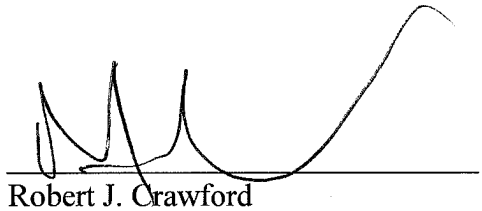
In view of the above, Appellant submits that the rejections of claims 1-15 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 

Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.593PA)

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/563,995)

1. Apparatus comprising an input stage with an NMOS transistor doublet having a first differential input for receiving input signals, a PMOS transistor doublet having a second differential input for receiving input signals, and a plurality of switches for receiving and selectively directing analog input signals only to one of either said first differential input or to said second differential input responsive to a switching signal and for connecting the other one of the first and second differential inputs to a reference voltage responsive to the switching signal, whereby the input stage is configured to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant.

2. The apparatus of claim 1, wherein the plurality of switches-direct the analog input signals to said first differential input if the input signals have positive gamma data and to said second differential input if the input signals have negative gamma data.

3. The apparatus of claim 1, wherein the NMOS transistor doublet comprises two NMOS transistors, each having a gate, whereby the gate of the first of the two NMOS transistors is connectable to a first input node via a first switch of the plurality of switches and the gate of the second of the two NMOS transistors is connectable to a second input node via a second switch of the plurality of switches, the PMOS transistor doublet comprises two PMOS transistors, each having a gate, whereby the gate of the first of the two PMOS transistors is connectable to the first input node via a third switch of the plurality of switches and the gate of the second of the two PMOS transistors is connectable to the second input node via a fourth switch of the plurality of switches.

4. The apparatus of claim 3, wherein the gate of the first of the two NMOS transistors is connectable, via a fifth switch of the plurality of switches, to a first reference node being biased with a first reference voltage, and the gate of the second of the two NMOS transistors is connectable to the first reference node via a sixth switch of the plurality of

switches, and the gate of the first of the two PMOS transistors is connectable, via a seventh switch of the plurality of switches, to a second reference node being biased with a second reference voltage and the gate of the second of the two PMOS transistors is connectable to the second reference node via an eighth switch of the plurality of switches.

5. The apparatus of claim 1, wherein the input stage is a rail-to-rail input stage.

6. The apparatus of claim 4, wherein the input stage is configured to keep the NMOS doublet active when the analog input signals are directed to the second differential input and to keep the PMOS transistor doublet active when the analog input signals are directed to the first differential.

7. The apparatus of or claim 1, wherein said switching signal is a digital switching signal.

8. The apparatus according to claim 1, wherein transistors serve as the switches.

9. The apparatus of claim 1 wherein the NMOS transistor doublet and the PMOS transistor doublet are part of a folded cascode rail-to-rail input stage and wherein the folded cascode rail-to-rail input stage is connected to a second stage comprising a rail-to-rail output stage amplifier.

10. Apparatus comprising a source driver bank with a plurality of apparatus according to claim 1, and further comprising a bus for receiving input signals.

11. The apparatus of claim 10, further comprising a gate driver bank and an LCD panel.

12. The apparatus of claim 10, further comprising a control signal generator for generating the switching signal.

13. The apparatus of claim 10 being part of a panel module.

14. The apparatus of claim 1, wherein the input stage is configured to operate in either a first mode or a second mode responsive to the switching signal, and the NMOS and PMOS transistor doublets are both kept active in each of the modes, and wherein the plurality of switches are configured, in the first mode, to direct the analog input signals to the first differential input and to connect a first reference voltage to the second different input, and the plurality of switches are configured, in the second mode, to direct the analog input signals to the second differential input and to connect a second reference voltage to the first differential input.

15. The apparatus of claim 1, wherein the first differential input is formed by the gates of the NMOS transistor doublet and the second differential input is formed by the gates of the PMOS transistor doublet.
image current in the tilling structures by a current in the inductive element.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.